Switching Characteristics of Nanowire Feedback Field-Effect Transistors with Nanocrystal Charge Spacers on Plastic Substrates

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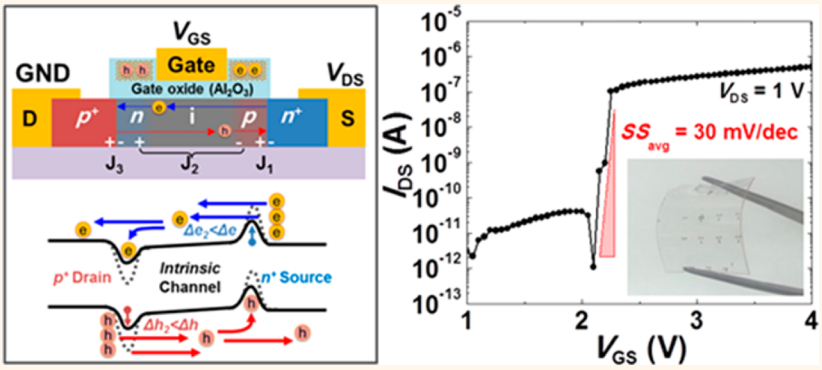
ABSTRACT



In this study, we demonstrate the abruptly steep-switching characteristics of a feedback field-effect transistor (FBFET) with a channel consisting of a p^+—i—n^+ Si nanowire (NW) and charge spacers of discrete nanocrystals on a plastic substrate. The NW FBFET shows superior switching characteristics such as an on/off current ratio of $\sim 10^5$ and an average subthreshold swing (SS) of 30.2 mV/dec at room temperature. Moreover, the average SS and threshold voltage values can be adjusted by programming. These sharp switching characteristics originate from a positive feedback loop generated by potential barriers in the intrinsic channel area. This paper describes in detail the switching mechanism of our device.

KEYWORDS: subthreshold swing · silicon nanowires · feedback loop · field-effect transistor · plastic substrate

Over the past four decades, the enormous development in complementary metal—oxide—semiconductor (CMOS) technology has led to great evolution in information technology. The continuous down-scaling of metal—oxide—semiconductor field-effect transistors (MOSFETs) has enabled tremendous improvement in switching speed, functionality, density, and manufacturing costs. However, power dissipation of the MOSFETs in the nanoscale regime has become a major problem in recent years because of their practical and theoretical limits.[1] To deal with the power dissipation problem of MOSFETs, numerous studies have focused on reducing the subthreshold swing (SS), which is defined as the gate voltage variation required to change the drain current by 1 order of magnitude in the subthreshold region of a transistor.[2,3] A reduced SS lowers the off-state current of a device under the same threshold voltage. Conventional MOSFETs have a theoretical limit of 60 mV/dec SS at room temperature owing to the nonscalability of their thermal voltage.[4,5] Therefore, device concepts are required to overcome the theoretical limit of the SS.

Recently, various promising transistor design approaches have been proposed and demonstrated to achieve SS values lower than the theoretical limit of MOSFETs. The tunneling FET (TFET)[5−11] and impact-ionization MOSFET (i-MOSFET) devices[12−18] have demonstrated SS values smaller than 60 mV/dec *via* band-to-band tunneling (BTBT) and avalanche breakdown, respectively. Moreover, an absolute zero SS value has been achieved by the abrupt movement

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of a mechanical gate electrode for nanoelectromechanical FETs (NEMFETs).[19,20] However, these designs suffer from some major drawbacks in the device applications. For the TFETs, the point SS rapidly increases as the device is turned on, and the on-current and the on−off current ratio (I_{on}/I_{off}) are relatively low. For the i-MOSFETs, a relatively higher operating voltage is necessary to generate an avalanche breakdown in the channels. Finally, for the NEMFETs, the device structure is very complicated, and mechanical stability cannot be guaranteed.

Feedback FETs (FBFETs) have been proposed by the C. Hu group as one of the promising candidates for next-generation switching devices[21,22] to overcome the major drawbacks experienced by the TFETs, i-MOSFETs, and NEMFETs. The basic structure of FBFETs is a trigated p^+-i-n^+ diode that uses Si/oxide−nitride−oxide/Si (SONOS) gate sidewall spacers on silicon-on-insulator (SOI) substrates. On the basis of the forward bias, steep SS characteristics of FBFETs can be easily achieved by trapping charges at the gate sidewalls. After sufficient charges are stored in the gate sidewall spacers, the band diagram of the FBFETs is modulated as a p−n−p−n structure. The modulated band-diagram structure of the FBFETs is similar to that of a thyristor[23] or a field-effect diode,[24,25] which shows the steep-switching characteristics owing to their positive feedback loop. Therefore, low SS characteristics, high I_{on}/I_{off}, and low-voltage operating characteristics can be realized in FBFETs. This FBFET positive feedback loop can be achieved with the help of proper device designs and charge-trap materials. Nevertheless, archiving trigate structures with SOI substrates is difficult because of the complicated fabrication steps. Hence, we propose the use of nanowires (NWs) as FBFET channels in this study to enable simple fabrication of the trigate of a gate-all-around (GAA) structure without resorting to any complicated methods. Moreover, NWs can be easily transferred onto plastic substrates to realize plastic electronics.[26,27] In the present study, we also propose the use of metal nanocrystals (NCs) as FBFET gate sidewalls to enhance the charge-trap characteristics with discrete structures and large work function of metal NCs. Therefore, the development of FBFETs with NWs and metal NCs becomes the most attractive research area. The electrical characteristics of an FBFET constructed on a plastic substrate with a p^+-i-n^+ Si NW and sputtered NC charge spacers are investigated in this work.

RESULTS AND DISCUSSION

Figure 1a shows the schematic device illustration and optical images of a Si NW FBFET on a plastic substrate. A p^+-i-n^+ Si NW with an intrinsic region length of 4 μm is used as an active channel material, and the platinum NC charge spacers located at both sides of the gate electrode regions are the discrete charge storage nodes with a width of 1 μm. Because the NW FBFET is constructed on a transparent plastic substrate, most of the device area is almost transparent, except for the electrodes. In addition, the use of the plastic substrate enables realization of a flexible switching device. Figure 1b shows the 2-D schematic device illustration and the energy band diagram of the FBFET in the off-state, *i.e.*, gate voltage (V_{GS}) = 0 V and drain voltage (V_{DS}) = 0 V. The device structure exhibits a forward-biased p^+-i-n^+ diode with a partial gate electrode arranged in the middle of the intrinsic region and the NC charge spacers located at the ungated intrinsic regions (at both sides of the gate electrode). Basically, the drain current (I_{DS}) of the forward-biased p^+-i-n^+ diode primarily depends on V_{DS}. However, I_{DS} of the FBFET is controlled by V_{GS} because of the presence of potential barriers at the intrinsic region. These potential barriers are generated by the charge carriers trapped at the NC charge spacers, namely, the holes trapped at the NC charge spacer located next to the p^+ drain region and the electrons trapped at the other NC charge spacer located next to the n^+ source. This state is called "programming". Figure 1c shows the cross-sectional SEM image of the p^+-i-n^+ Si NW on a bulk Si substrate taken after crystallographic wet etching, size-reduction oxidation, and masked ion implantation. To distinguish the NWs from the surrounding oxide layer, poly-Si deposition and chemical staining using buffered-oxide-etch solution are performed before their SEM images are taken. The NW is formed with an inverted-triangle shape during the crystallographic wet etching because of the different etching ratios of the (110)- and (111)-Si planes using a tetramethylammonium hydroxide (TMAH) solution. The NW diameter after the crystallographic wet etching and thermal oxidation process are completed is ~100 nm. Compared with the planar structure, the use of NWs for the switching device can extend the gate coverage, such as in an omega-gate-shaped structure, without employing any complicated fabrication step on the plastic substrate. Therefore, we expect that the NW-based switching devices can exhibit much improved electrical characteristics compared with the planar-structure-based devices. The cross-sectional HRTEM image of the NC charge spacers embedded at the ungated intrinsic regions of the NW FBFET is shown in Figure 1d. The platinum NCs with an average size of approximately 3−5 nm are separated from one another. The platinum NCs were formed on the gate layer via the nucleation and growth of islands of platinum atoms during the dc magnetron sputtering process (see Supporting Information).With a large platinum work function (~5 eV), the NC charge spacers show good charge-trap characteristics, including higher storage capacity and improved charge retention, compared with the other spacer materials such as silicon nitride.[28−30]

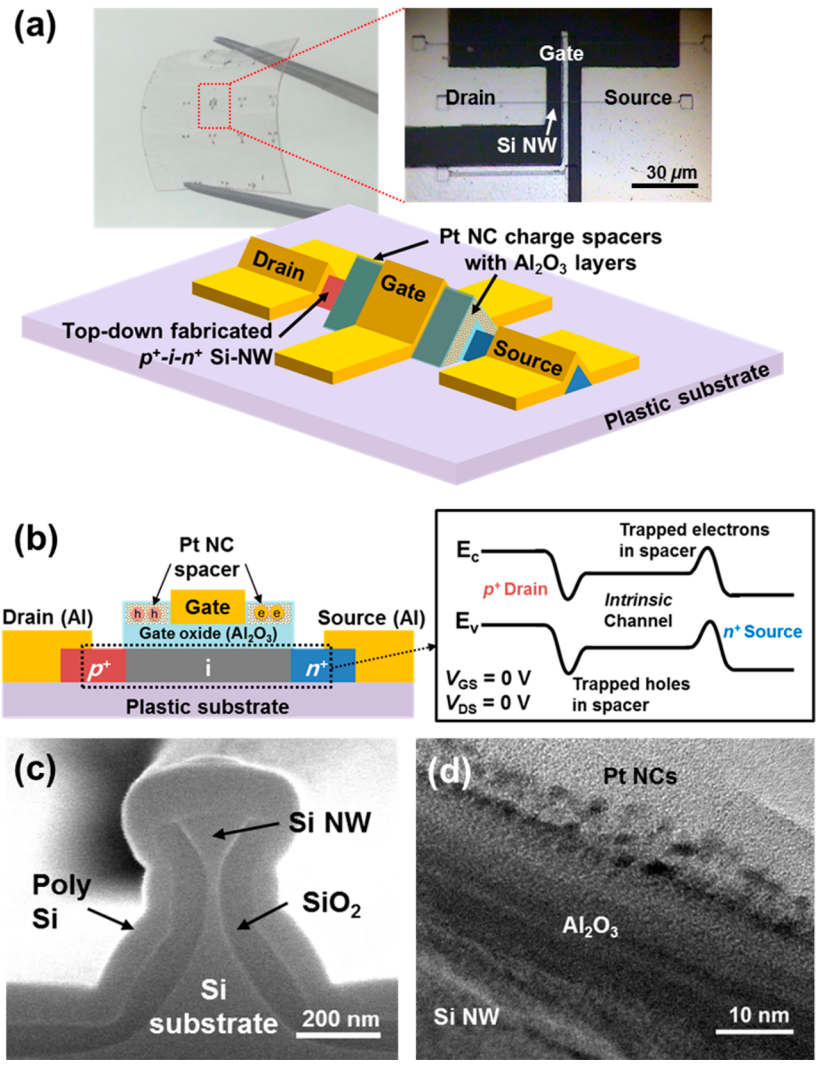

Figure 1. (a) Schematic illustration and optical images of the NW FBFET on a plastic substrate. (b) 2-D device structure and energy band diagram of the FBFET in the off-state (V_{GS} = 0 V, V_{DS} = 0 V). (c) Cross-sectional SEM views of the p^+–i–n^+ Si NWs on a bulk Si substrate. (d) Cross-sectional HRTEM images of the NC charge spacers embedded in the ungated intrinsic regions of the NW FBFET.

We investigate the electrical characteristics of the NW FBFET operated as an n-channel device on the plastic substrate. Figure 2a shows the diode voltage *versus* diode current characteristics of the p^+–i–n^+ Si NW for the FBFET without any gate bias. The diode exhibits typical rectifying properties. The ideality factor of the diode is estimated to be ~2.47, which is relatively small, indicating that the p^+–i–n^+ Si NWs have abrupt junction profiles. The I_{DS} *versus* V_{GS} characteristics at V_{DS} = 1 V for the NW FBFETs are shown in Figure 2b. The I_{DS} *versus* V_{GS} curves are obtained after the programming at V_{GS} = −10 V and V_{DS} = 1 V for 1 s. After the programming, one NC charge spacer located next to the p^+ drain region is positively charged, and the other NC charge spacer located next to the n^+ source region is negatively charged. The device shows an abruptly steep-switching behavior with I_{on}/I_{off} of ~10^5 and an extracted threshold voltage (V_{TH}) of 2.25 V. In the subthreshold region, the average SS value, defined as the change in the gate voltage *versus* the logarithmic values of the drain current from the off-state voltage to the threshold voltage,[31] is estimated to be 30.2 mV/dec, which is below the theoretical limit of 60 mV/dec of MOSFETs at room temperature. To confirm the steep-switching behavior that originates from the NC charge spacers of the NW FBFET, a gated p^+–i–n^+ diode without any NC charge spacers is also prepared as a reference device. The inset in Figure 2b shows the V_{GS} *versus* I_{DS} characteristics obtained from the reference device. Under the same programming and the same measurement conditions, the reference device does not exhibit any switching properties, which indicates that the NC charge spacers, which generate the potential barriers at the intrinsic channel in the NW FBFET, have a significant influence on the switching characteristics. Moreover, the point SS value, defined by the simple expression SS = $dV_{GS}/d(\log 10|I_{DS}|)$, is extracted as a function of V_{GS}, as shown

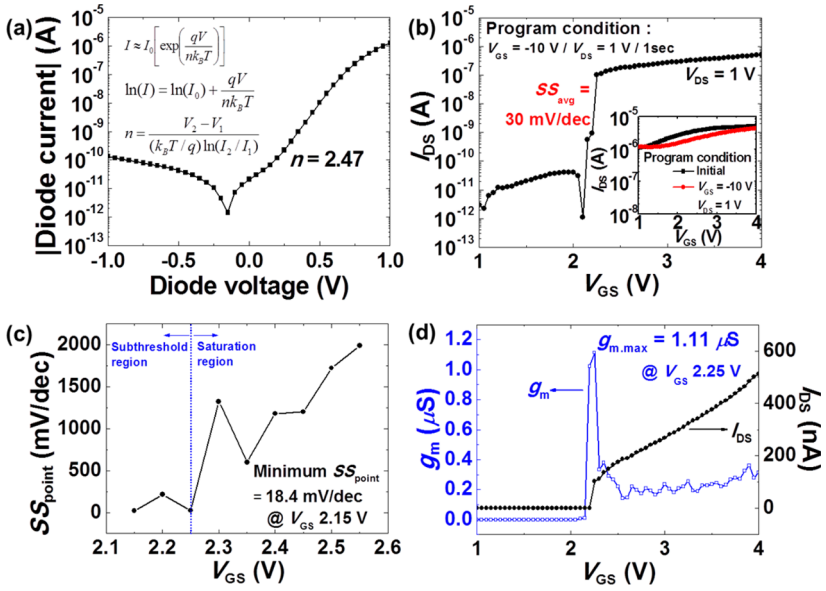

Figure 2. (a) Diode voltage *versus* diode current characteristics without any gate bias. (b) V_{GS} *versus* I_{DS} characteristics of the NW FBFET at V_{DS} = 1 V after the programming at V_{GS} = −10 V and V_{DS} = 1 for 1 s. The inset shows the V_{GS} *versus* I_{DS} characteristics of the gated p^+−i−n^+ diode without any NC charge spacers. (b) Change in the point SS value as a function of V_{GS} of the NW FBFET operated as an n-channel device. (c) Transconductance obtained from the NW FBFET at V_{DS} = 1 V. The linearly scaled V_{GS} *versus* I_{DS} curve is included for comparison.

in Figure 2c. In the subthreshold region, the minimum value of the point SS is estimated to be 18.4 mV/dec at V_{GS} = 2.15 V, which corresponds to a significantly low point SS value. When the device shows the steep-switching characteristics, the transconductance value (g_m) abruptly increases. Figure 2d shows the V_{GS} *versus* g_m characteristics obtained from the NW FBFET at V_{DS} = 1 V. For comparison, the linearly scaled V_{GS} *versus* I_{DS} curve is shown in Figure 2d. The maximum g_m value is 1.11 μS at V_{GS} = 2.25 V. However, when V_{GS} is above 2.25 V, the g_m value decreases and shows the saturated characteristics.

The SS characteristics of the NW FBFET are investigated under different programming conditions. The I_{DS} *versus* V_{GS} characteristic and the point SS values of the NW FBFET at the initial state and after the programming (with V_{GS} = −10 V and V_{DS} = 1 V for 1 s) are shown in Figure 3a and c. The initial state is set by keeping the device under vacuum for 7 days to remove the charges at the NC charge spacers. In the initial state, the I_{DS} *versus* V_{GS} curve shows a gradual slope with an average SS value of 281 mV/dec and a minimum point SS value of over 100 mV/dec. After the programming is applied, the average and minimum point SS values remarkably improve. The average SS value is 49.7 mV/dec. Moreover, the minimum point SS value is 28.5 mV/dec, and low point SS values are maintained in the subthreshold region, as shown in Figure 3c. Additionally, V_{TH} shifts from 2.95 to 1.45 V. The I_{DS} *versus* V_{GS} curves and point SS values obtained after the programming at V_{GS} = +10 V and V_{DS} = 1 V or at V_{GS} = −10 V and V_{DS} = 1 V are shown in Figure 3b and d; the programming time is 1 s. In the I_{DS} *versus* V_{GS} curves, the average SS changes from 262 to 59.2 mV/dec, and the minimum point SS changes from 101 to 40.1 mV/dec. Further, V_{TH} shifts from 2.75 to 1.75 V. The significant V_{TH} shift indicates the potential application of the NW FBFET to nano-floating gate memory devices or flash memories.[32] The injection of charge carriers between the channel and the charge spacer by the programming causes both the shift in V_{TH} and the generation of the positive feedback loop. The high I_{on}/I_{off}, the sub-60 mV/dec SS, and the wide V_{TH} transition demonstrate that the NW FBFETs offer a clear potential for not only steep-switching devices but also high-performance memory devices.

Unlike the BTBT of the TFETs or impact ionization of the i-MOSFETs, the basic operating principle of the FBFET can be explained on the basis of a positive feedback loop at the intrinsic channel area; a more detailed mechanism of the feedback loop in our FBFET is described in the Supporting Information. The schematic energy band diagrams of the positive feedback loop of the n-channel FBFET are shown in Figure 4. After the programming, the FBFET band diagram is similar to that of a p^+−n−i−p−n^+ structure; the n−i−p virtual doping at the channel is induced by the charge carriers trapped at each of the NC charge spacers. Although a forward bias is applied through the source to the drain, the FBFET remains in the off state because of the reverse-bias state at the channel. Therefore, the off-state current can be regarded as a reverse junction leakage current. After V_{GS} increases, the height of the potential barrier located near the n^+ source decreases; thus, electrons can be injected to the channel. Some of the injected electrons flow toward the p^+ drain, and the others accumulate at the

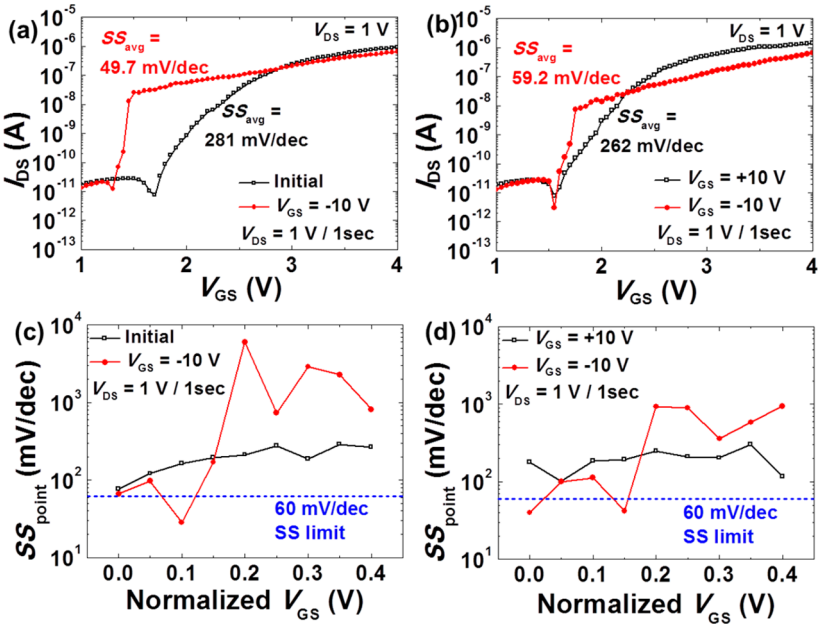

Figure 3. V_{GS} *versus* I_{DS} curves of the NW FBFET at V_{DS} = 1 V (a) for the initial state and after the programming at V_{GS} = −10 V and V_{DS} = 1 and (b) after the programming at V_{GS} = +10 V and V_{DS} = 1 or at V_{GS} = −10 V and V_{DS} = 1. All programming processes are performed for 1 s. (c and d) Variation in the point SS values as normalized V_{GS} values of the NW FBFET with individual programming condition. We note that the V_{GS} values with the lowest I_{DS} from each V_{GS} *versus* I_{DS} characteristics are normalized to 0 V.

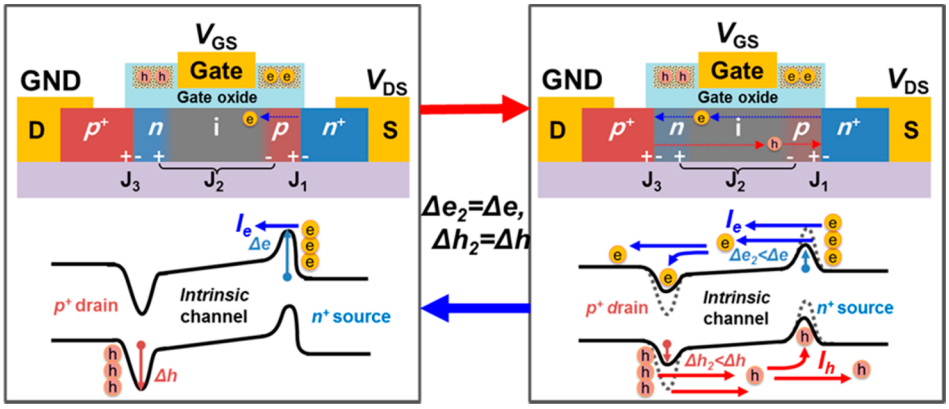

Figure 4. Schematic energy band diagrams of the positive feedback loop of the FBFET for an n-channel operation.

opposite potential well. Then, the accumulated electrons lower the height of the potential barrier located near the p^+ drain. The lowering of the potential barrier located near the p^+ drain allows the holes to flow from the p^+ drain to the channel. Some of the injected holes also accumulate at the potential well located near the n^+ source, leading to the lowering of the potential barrier located near the n^+ source, which results in electrons being injected to the channel. In other words, the lowering of the potential barrier height recursively occurs because of the accumulation of the injected charge carriers at the potential well. Therefore, the lowering of the heights of both potential barriers generates positive feedback amplification in the device channel.

In Table 1, the switching characteristics of our FBFET are compared with those of the switching devices previously reported by other research groups. For the TFETs, the point SSs have relatively small values of 30−50 mV/dec, which are directly related to the BTBT efficiency. The BTBT barrier should be thin enough for the charge carriers to easily tunnel through it. Therefore, extremely small channel diameter, high-k dielectrics, channel band gap, and abrupt junction profiles are required to achieve steep SSs for the TFETs. Nevertheless, the average SS values are relatively large (over 50 mV/dec) because the BTBT efficiency worsens as the drain current increases. For the i-MOSFETs, impact ionization can be effectively generated on the basis of the thin and short channel device structure. Therefore, thin SOI- or NW-based i-MOSFETs show very steep SS values (3−20 mV/dec). Nevertheless, the need for high operating voltages (~17.5 V) to generate impact ionization is inappropriate for steep SS devices at

TABLE 1. Electrical Characteristic Comparison for the Steep Subthreshold Switching Devices

ref	device	technology	SS at 300 K (mV/dec)	$\|V_{ds}\|$ (V)	I_{on}/I_{off}	year
8	TFET	vertical Si NW, GAA	30−50 ($point_{min}$)	0.6	$\sim10^6$	2011
9	TFET	vertical Si NW	∼30 ($point_{min}$) ∼50 (av)	1.2	$\sim10^5$	2011
10	TFET	SOI, omega-gate, strained Si	76 ($point_{min}$) 97 (av)	0.3	$\sim10^6$	2012
15	i-MOS	SOI, planar	3.7 (av)	6.5	$\sim10^6$	2005
17	i-MOS	SOI, planar Si oxide	20 ($point_{min}$)	17.5	$\sim10^5$	2007
18	i-MOS	multiple gate, strained SiC NW	∼5 (av)	5.75	$\sim10^4$	2008
21	FBFET	SOI, FinFET	∼40 (av)	1.2	$\sim10^7$	2008
this work	FBFET	SiNW, plastic substrate	18.4 ($point_{min}$) 30.2 (av)	1	$\sim10^5$	2013

low-power operation. In contrast, for the FBFETs, the positive feedback loop generates an exponential increase in the electron and hole current at the channel area, which results in steep SS characteristics. This positive feedback loop does not require high operating voltages or complicated device structures. Moreover, the triggering of the positive feedback loop can be controlled by adjusting the height of the potential barriers. In addition, the FBFET off-current can be defined as a reverse junction leakage current, which has a substantially low value compared with the off-current (generated by thermal injection) in conventional MOSFETs. The forward-biased V_{DS} provides a relatively high on-current magnitude. In particular, our device realizes steep-switching properties using Si NW on a plastic substrate. The use of NWs on the plastic substrates easily realizes a broadened gate coverage of the device, which can realize enhanced controllability of the channel area covered by the gate electrode without resorting to any complicated fabrication process, Moreover, compared with the bulk or SOI substrate-based devices, our device on a plastic substrate offers possibilities for transparent and flexible steep-switching devices. With the application of this unique operating principle and the simple device structure of FBFETs with NWs, substantially lower SS values and relatively higher on/off current ratios can be achieved in principle.

CONCLUSIONS

In summary, we have demonstrated the switching characteristics of an FBFET with a p^+−i−n^+ Si NW and NC charge spacers on a plastic substrate. The switching characteristics include an I_{on}/I_{off} of $\sim10^5$, an average SS value of 30.2 mV/dec, a minimum point SS of 18.4 mV/dec, and a maximum g_m of ∼1.11 μS. Excellent switching characteristics are achieved by the positive feedback loop. The feedback loop operates by controlling the height of the potential barriers generated by the charges trapped in the NC charge spacers at the intrinsic channel area. Furthermore, the wide V_{TH} transition indicates that the FBFET can operate as a promising memory device. The present study opens the possibilities of NW-based steep-switching devices with sub-60 mV/dec SS for future plastic low-power electronics.

EXPERIMENTAL SECTION

Device Fabrication. First, p^+−i−n^+ Si NWs were fabricated from a (100)-orientation bulk-Si wafer (doping concentration ≈ 10^{16} atoms/cm^3) by a CMOS-compatible top-down process, which includes conventional photolithography, crystallographic wet etching with a TMAH solution, thermal oxidation, and masked ion implantation.[33] The doping concentration of the p^+ drain/n^+ source regions was $\sim10^{20}$ cm^{-3}. The NWs were then transferred onto a polyethersulfone plastic substrate *via* direct transfer method.[34] The Al source, drain, and gate electrodes were patterned by photolithography and then deposited *via* thermal evaporation. The source/drain contact electrodes were formed with thermally deposited Al metal, and an Al_2O_3 gate-oxide layer with a thickness of ∼15 nm was formed using atomic layer deposition. The 2-μm-wide Al gate electrode was then aligned in the middle of the intrinsic NW channel. After the regions of the platinum NC charge spacers were defined, platinum NC charge spacers were formed on the gate layer *via* a dc magnetron sputtering process; accelerated Ar^+ ion gas molecules out of plasma hit a platinum target. Then platinum atoms are detached from the target and deposited on a substrate. These single atoms create nuclei, and they then grow into islands. The islands continue to coalesce, and finally the formation of NCs takes place. The platinum NCs were deposited for 8 s with the sputtering conditions of an Ar gas pressure of 3 mTorr, a sputtering power of 25 W, and a substrate temperature of 290 K. All the fabrication processes except the Si NW fabrication were conducted on the plastic substrate, and all the process temperatures did not exceed 150 °C.

Measurement. All electrical data were taken using a semiconductor-parameter analyzer (HP4155C, Agilent) at room temperature. The morphologies of the NWs on the bulk-Si wafer and the platinum NC charge spacers were examined using scanning electron microscopy (SEM: S-4300, Hitachi) and high-resolution transmission electron microscopy (HRTEM: Tecnai G2 F30, FEI), respectively.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The physical mechanism of the Pt nanocrystal formation *via* dc magnetron sputtering process and operating mechanism of NW FBFETs based on the standard thyristor modeling. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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